IN SITU MICROWAVE CHARACTERIZATION OF INSULATOR THIN FILMS FOR INTERCONNECTS OF ADVANCED CIRCUITS

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ABSTRACT

An accurate and simple method to in-situ characterize the dielectric constant of insulator thin films is developed. Optimized devices under test are capacitive patches where insulator film is set in the future operational configuration. Dielectric constant is extracted by an optimization procedure based upon subnanosecond time domain reflectometry measurement and simulation. ε_r is given into a 100 MHz - 10 GHz frequency bandwidth.

INTRODUCTION

Thermal and electrical performances of advanced microwave or high speed circuits are strongly dependent on used materials [1,2]. In order to improve performances due to interconnection network in such circuits, new materials combined to thin film technologies are elaborated [3]. For example, new SiOF or TEOS insulator oxides show promising low dielectric constant and deposition process facilities. However, for designers, in-situ electrical material characteristics, as the permittivity of insulator layers, must be known in the future operational configuration, i.e. after deposition and etching process steps and with the presence of conductive layers. Next upon these characterization results and regarding the process control, design rules and electrical parameters of materials can be optimized to improve performances of interconnections, as low attenuation and low delay [4].

We have developed an accurate and simple method for an in-situ measurement of the real part of insulator thin film permittivity. This method is distinguished by the following properties :

- Specific devices under test (DUT) are easily processed,
- Theoretical approach uses a simple and a phenomenological lumped electrical equivalent circuit of the DUT, where circuit elements are given by accurate analytical formulas,
- Measurements are fast and performed by a Time Domain Reflectometry technique (TDR),
- Dielectric constant extraction procedure is easily performed by comparison between time measurements and SPICE simulations of the equivalent circuit.

Accuracy on the dielectric constant determination is about 4% into a MHz-GHz frequency bandwidth.

DEVICES UNDER TEST STRUCTURE

Fig. 1 shows a typical cross-section of the multilayered configuration from which the DUT must be realized. The insulator thin film under test of about h=500 nm thickness is sandwiched between two AlCu metallic alloy layers of about t=500 nm thickness. The overall layers are deposited onto a Si-substrate and isolated by using a e=410 nm-thick SiO_2 oxide layer. DUT are depicted in fig. 2.

Three contact pads are designed on the AlCu metallic top layer to connect the DUT to a 50 Ω

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coplanar probe (150 μm pitch). External pads are jointed to the AlCu metallic ground plane by a via hole. A large capacitive patch is also designed on the top surface and connected to the middle probe pad through a short microstrip line of 10 μm-width and 300 or 500 μm-length. Geometrical parameters of DUT are resumed in table 1.

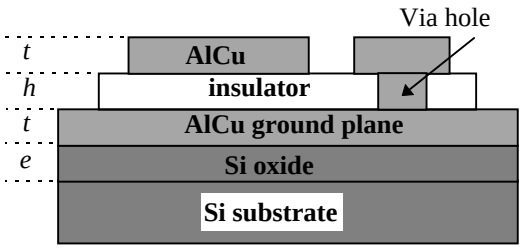

Fig. 1 : Typical cross-section of investigated multilayer structures on SiOF and TEOS insulators.

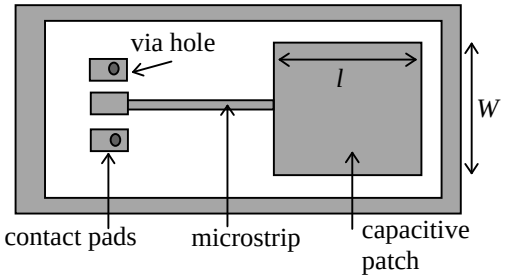

Fig. 2 : Top view of DUT.

insulator SiOF	insulator TEOS	patch		
		l (μm)	*W* (μm)	area (mm^2)
h=530nm	h=470nm	450	380	S_1=0.171
		800	500	S_2=0.4
		500	800	S'_2=0.4
		1700	1000	S_3=1.7
		2850	1500	S_4=4.275

Table 1 : Description of DUT.

MEASUREMENT TECHNIQUE

TDR measurement system is described in fig. 3. A digital sampling oscilloscope Tektronix CSA803A with SD24 sampling-head generator is connected to the DUT through a low loss 50 Ω cable and a Cascade Microtech probe head. The SD24 sampling-head includes a 500 mV step-like pulse generator of about 18 ps risetime and a feedthrough sampling-head of 20 GHz bandwidth.

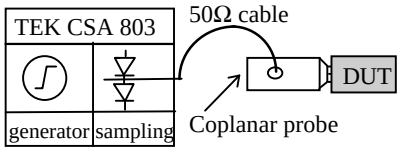

Fig. 3 : TDR measurement system.

DUT EQUIVALENT CIRCUIT

A similar and simplified approach of the technique presented in [5] is used. Equivalent circuit of the DUT is assumed a lumped circuit because the length of the DUT is short compared to the signal wavelength into the investigated frequency bandwidth, up to a few of GHz. As first approximation, the DUT equivalent circuit can be a simple lumped *RC* circuit, but this model has been inadequate to extract the insulator dielectric constant. As second approximation, modeling of each section of DUT, *i.e.* pads, microstrip, and patch, can be a lumped *R, L, C, G* circuit. In addition, each section can be assumed to be a parallel plate waveguide because the width of conductive layers are large compared to the insulator thickness (*W/h>20*). Such assumptions allow to calculate lumped element values, in each section, by [6] :

$$R = \frac{2l}{\sigma W t}\ ,\ L = \mu_o \frac{l}{W}\left(h + \frac{2t}{3}\right)$$

$$C = \varepsilon_o \varepsilon_r \frac{Wl}{h}\ ,\ G = \varepsilon_o \varepsilon_r \frac{Wl}{h}\omega \tan\delta$$

where ε_r, $\tan\delta$ and h are respectively dielectric constant, dielectric loss and thickness of insulator, and σ, t, l, W are respectively conductivity, thickness, length and width of conductors.

Up to a few of GHz, skin effect is insignificant on R and L, but internal inductance effect is taken into account. As $W>>h$ fringing fields can be neglected in C and G. Using results of a sensitivity study, equivalent circuit of the DUT is presented in fig. 4.

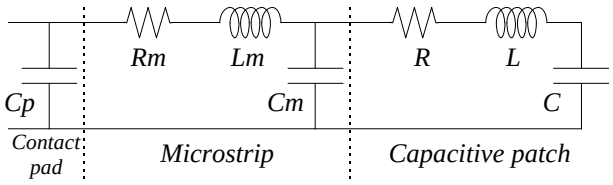

Fig. 4 : DUT electrical equivalent circuit.

RESULTS

Extraction of dielectric constant real part is performed by an iterative optimization technique. We use the minimization of an error function directly based upon the deviation between simulated and measured time reflected signals. Electrical simulations are performed by Spice using a simulated incident signal similar to the TEK SD24 generator signal. The error function is given by an estimation of the mean quadratic deviation :

$$e = \sqrt{\frac{1}{N}\sum_{i=1}^{N}\left|V_m(t_i)\right|^2 (1-\zeta^2)}$$

$$\text{with } \zeta = \frac{\sum_{i=1}^{N} V_m(t_i)V_s(t_i)}{\sqrt{\sum_{i=1}^{N}\left|V_m(t_i)\right|^2 \sum_{i=1}^{N}\left|V_s(t_i)\right|^2}}$$

where $V_m(t_i)$ is measurement of the reflected voltage at the time t_i, $V_s(t_i)$ is the simulated reflected voltage at t_i, and N is the number of test points (i=1 to N=30) in the reflected voltage response.

Because AlCu layer conductivity has been measured by a method of four probes (σ=33 10^6 S/m), parameters to be optimized are only capacitances C_p, C_m and C which are directly function of the insulator dielectric constant.

For capacitive patches of S_2=0.4 mm^2 area on SiOF and TEOS insulator films, measurements and optimized simulations of reflected voltages are given in fig. 5. Optimized simulations are in accordance with measurements. Error function between measurements and simulations has been minimized better than the value obtained with repeatability measurements.

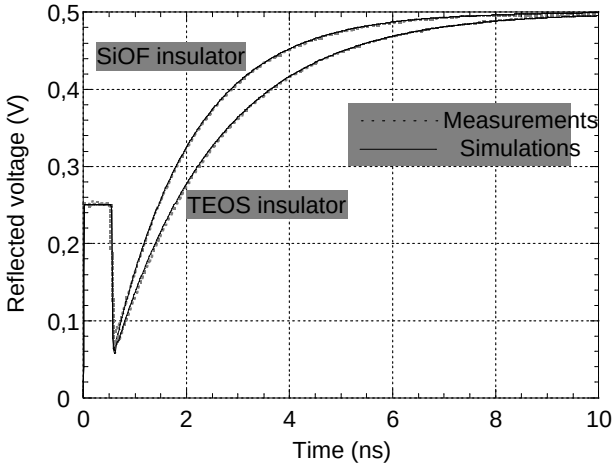

Fig. 5 : Measured and simulated reflected voltages for SiOF and TEOS insulators (patch area S2=0.4 mm^2)

Time-frequency transformations of TDR measured and simulated signals show that our method explores the dielectric constant, assumed constant in frequency domain, into the 100 MHz - 10 GHz bandwidth.

Measurements of TDR signals for different capacitive patch area shapes realized on SiOF and TEOS insulator thin films are given in fig. 6. We note that measured TDR signals, for example with S_2=800 x 500 mm^2 and S'_2=500 x 800 mm^2 patch areas are the same. So, step effects between the microstrip line and patch shape effects can be neglected.

After contact pads and 500 μm microstrip have equivalent circuit elements given by :

- with SiOF insulator :

C_p=560 fF, R_m=6 Ω, L_m=55.5 pH, C_m=309 fF

- with TEOS insulator :

C_p=744 fF, R_m=6 Ω, L_m=49.1 pH, C_m=450 fF.

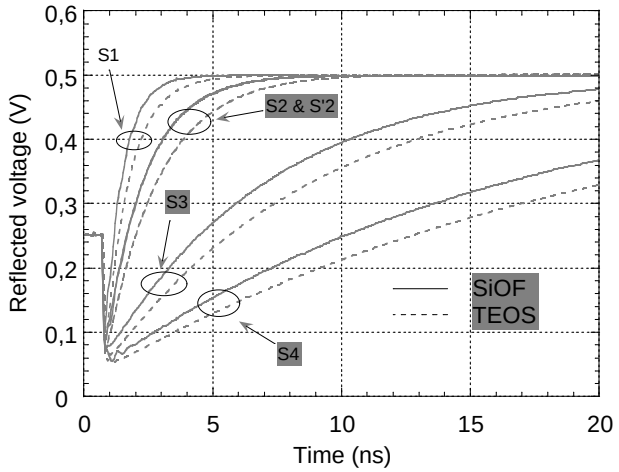

Fig. 6 : Measured TDR voltages for SiOF and TEOS insulators. S_i are DUT patch areas.

Extracted values of patch capacitances *C* are given in fig. 7 as a function of patch area. A very good linearity is obtained, in accordance with the plane capacitance model without fringing field effects. So, upon this model, fig. 7 shows also dielectric constant of SiOF and TEOS thin films as a function of patch area. Mean values of ε_r are ε_r=3.97 for SiOF and ε_r=4.86 for TEOS. Maximal deviation around these mean values are 2%. Accuracy on dielectric constant is directly related to the accuracy of insulator thickness, which about 2%. So, dielectric constant accuracy is better than 4%.

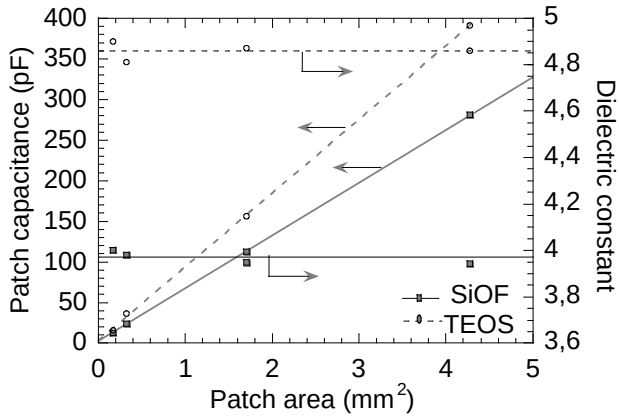

Fig. 7 : Extracted patch capacitance C and dielectric constant as a function of patch area.

CONCLUSION

A simple, fast and accurate method to in-situ characterize the dielectric constant of insulator thin films has been developed. TDR measurements are performed on specific large capacitive patches and compared to electrical simulations based upon an equivalent circuit. Dielectric constant is determined into a 100 MHz -10 GHz bandwidth and accuracy is about 4% assuming an insulator thickness uncertainty of 2%. This characterization can be useful for designers in order to perform and to supervise technological processes and circuit achievements.

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